MITSUMI

2024/12/23 Ver.1.0

Analog Front-End IC

MM3609ARRE Datasheet

FUNCTION

This IC is an Analog Front-End IC which changes analog signal output from a sensor to a digital signal, processes the digital signal, and outputs it to a host such as a microcomputer in the subsequent stage through digital communication. This corresponds to wide variety of sensors.

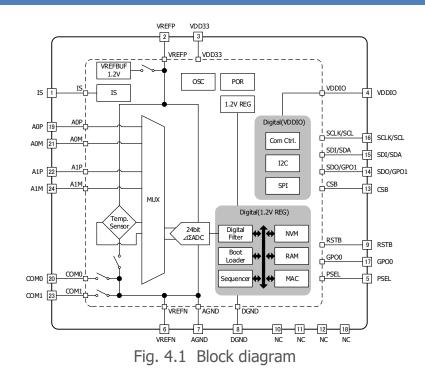
FEATURES

- · 24bit \angle 24b
- Able to store sensor-correcting sequence and corrective coefficient needed for correcting sensors in a non-volatile memory built in this IC. Correction is completed within this IC.
- · Selectable communication interface: I2C Hs (max. 3.4Mbps) or SPI4-wire (max. 5Mbps)
- Able to behave with low voltage of 1.71V or above
- · Temperature sensor is equipped. Able to correct temperature characteristics of external sensor
- · Effective resolution or data-output-rate is selectable to suit users.
- Equipped with a built-in oscillator. No external oscillation circuit is needed.
- · Corresponding to two modes of sensor driving method: constant current and constant voltage

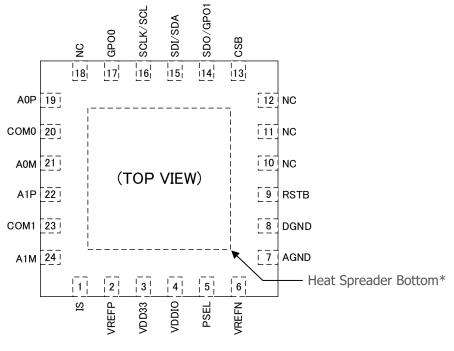
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BLOCK DIAGRAM



PIN LAYOUT





TERMINAL EXPLANATIONS

Pin function

Table 6.1 Pin list

No.	Name	TYPE	FUNCTION
1	IS	0	Output of constant current for driving external sensor
2	VREFP	I/O	Reference voltage plus *Internal VREF (=1.2V) is selectable by using sequence command.
3	VDD33	Ι	Power supply for analog circuit
4	VDDIO	Ι	Power supply for digital I/O
5	PSEL	Ι	Protocol select pin (High: SPI / Low: I2C)
6	VREFN	Ι	Reference voltage minus
7	AGND	-	Analog GND
8	DGND	-	Digital GND
9	RSTB	Ι	Negative logic reset
10	NC	Ι	*Inspection terminal: Do not connect
11	NC	I/O	*Inspection terminal: Do not connect
12	NC	Ι	*Inspection terminal: Do not connect
13	CSB	Ι	Chip select for SPI communication
14	SDO GPO1	0 0	Serial Data Output for SPI communication (SDO=MISO) *When I2C is selected: General-use output port 1
15	SDI	Ι	Serial Data Input for SPI Communication (SDI=MOSI)
16	SDA SCLK SCL	I/O I I/O	Serial Data Input and Output for I2C Communication (SDA) Serial Clock for SPI communication (SCLK) Serial Clock for I2C communication (SCL)
17	GPO0	0	General Purpose Output Port 0
18	NC	-	No connection
19	AOP	Ι	External sensor input signal plus: Channel 0
20	COM0	Ι	Pin for controlling external sensor ground: Channel 0
21	AOM	Ι	External sensor input signal minus: Channel 0
22	A1P	Ι	External sensor input signal plus: Channel 1
23	COM1	Ι	Pin for controlling external sensor ground: Channel 1
24	A1M	Ι	External sensor input signal minus: channel 1

Equivalent circuit of pins

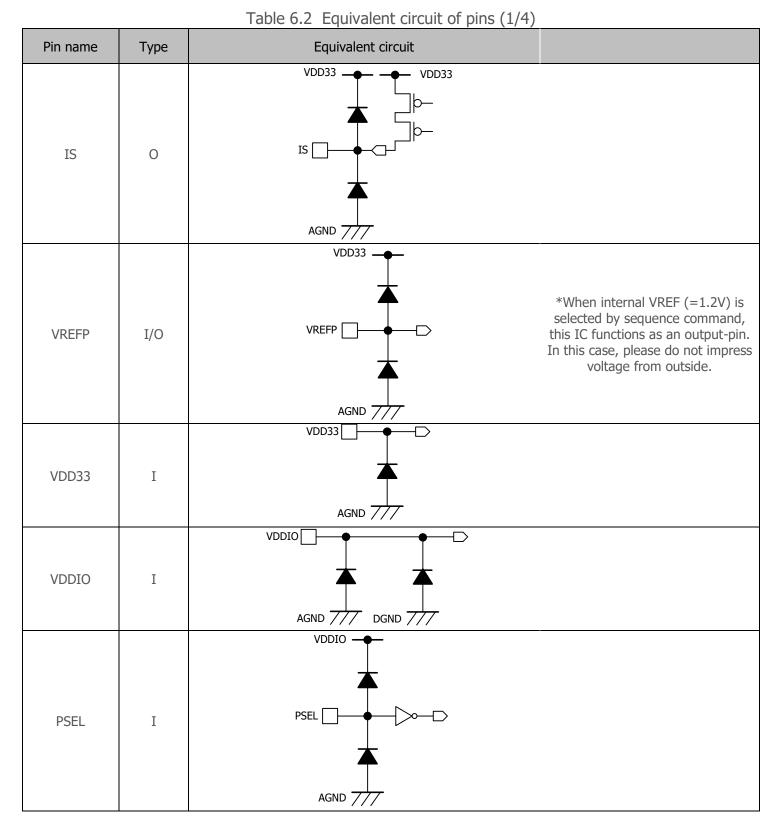
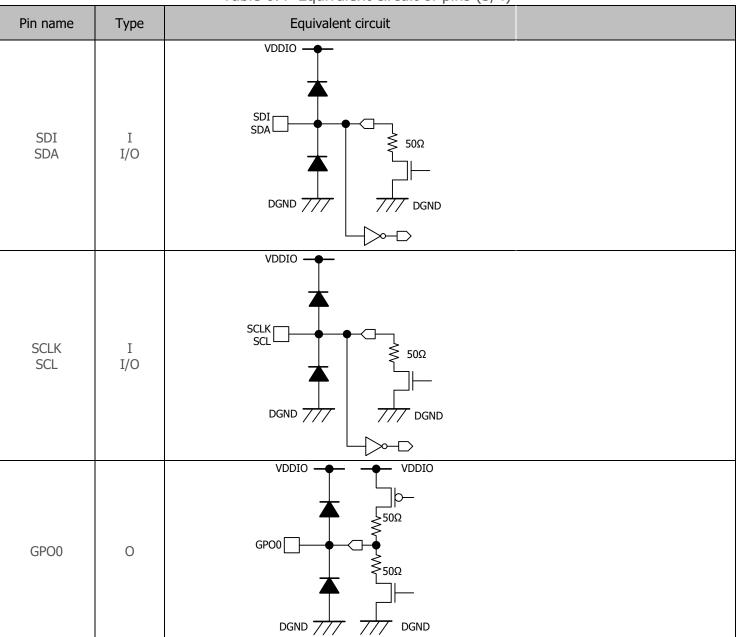


Table 6.3 Equivalent circuit of pins (2/4)					
Pin name	Туре	Equivalent circuit			
AGND VREFN	- I	_			
DGND	-	_			
RSTB	Ι	VDDIO VDIO VDDIO			
CSB	Ι				
SDO GPO1	0 0	VDDIO VDDIO VDDIO VDDIO VDDIO SDO GPO1 SDO SDO SDO SDO SDO SDO SDO SDO			



Pin name	Туре	Equivalent circuit
A0P A0M A1P A1M	I	VDD33 AOP AOM A1P A1M AGND ////
COM0 COM1	Ι	VDD33 COM0 COM1 Ron:TYP.25Ω AGND

Table 6.5 Equivalent circuit of pins (4/4)

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, Ta=25deg.C)

Item	Symbol	Min.	Max.	Unit
Storage temperature range	T _{STG}	-55	+105	deg.C
Analog power supply voltage	VDD33max	-0.3	+4.0 (note ¹) +6.1 (note ²)	V
Digital I/O power supply voltage	VDDIOMAX	-0.3	+4.0 +1.32 (note ² , note ³)	V

RECOMMENDED OPERATING CONDITIONS

(Unless otherwise specified, Ta=25deg.C)

Item	Symbol	Min.	Max.	Unit
Operating temperature range	T _{OPR}	-40 +10 (note ²)	+85 +30 (note ²)	deg.C
Analog power supply voltage	VDD33 _{OPR}	+1.71 +5.90 (note ²)	+3.60 +5.90 (note ²)	V
Digital I/O power supply voltage	VDDIO _{OPR}	+1.14 +1.14 (note ²)	+3.60 +1.32 (note ²)	V
Reference voltage	VREFPOPR	+1.14	VDD33	V
Differential input voltage	VID _{OPR}	-VREFP	+VREFP	V
Common mode input voltage	VICOPR	0	VDD33	V

note¹: Please do not exceed +4.0V during normal use (except NVM writing).

note²: During NVM writing

note³: Please do not exceed +1.32V during NVM writing.

· Power-on sequence

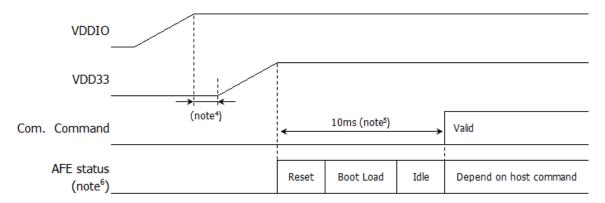


Fig. 8.2 Power-on sequence

- note⁴: No time is specified from starting VDDIO to input VDD33.
- note⁵: Communication shall not be started earlier than 10ms after starting both power sources of VDDIO and VDD33. Communication shall not be started earlier than 10ms after sending reset command. All commands ignore during Boot Load.
- note⁶: The above is Power-on sequence under the condition without NVM programming in IC. For the case with NVM programming, AFE status after Boot Load differs.

ELECTRICAL CHARACTERISTICS

Current consumption

(Unless otherwise specified, Ta=25deg.C, VDD33=VDDIO=3.3V)

Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Current consumption	IAD	at AD conversion	-	540	650	
	IADt	at AD conversion of temperature sensor inside IC	-	650	790	uA
Current consumption at shut down	Isd	at shut down	-	0.1	1.0	uA

Digital I/O

(Unless otherwise specified, Ta=25deg.C, VDD33=VDDIO=3.3V)

Item	Symbol	Condition	Min.	Тур.	Max.	Unit
H-level input voltage	VIH		0.8 × VDDIO	-	VDDIO + 0.3	V
L-level input voltage	VIL		-0.3	-	0.2 × VDDIO	V
Output voltage H-level	V _{OH1}	$VDDIO \ge 2.0V$ $I_{OH}=-3mA$	VDDIO – 0.4	-	-	V
	V _{OH2}	VDDIO < 2.0V $I_{OH}=-1mA$	0.8 × VDDIO	-	-	V
Output voltage L-level	Vol1	$\begin{array}{l} \text{VDDIO} \geqq 2.0\text{V}\\ \text{I}_{\text{OL}}=3\text{mA} \end{array}$	-	-	0.4	V
	V _{OL2}	VDDIO < 2.0V $I_{OL}=1mA$	-	-	0.2 × VDDIO	V
RSTB Low period (note ¹⁰)	t rstbl		10	-	-	US

note¹⁰: Design assurance items before correction

Current for sensor driving

(Unless otherwise specified, Ta=25deg.C, VDD33=VDDIO=3.3V)

Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Setting range of the current for sensor driving	Is		10	-	1270	uA
Setting Steps of the current for sensor driving	Isstep		-	10	-	uA
Allowable error of the current for sensor driving	Iserror		-7	-	+7	%

Reference voltage inside IC

(Unless otherwise specified, Ta=25deg.C, VDD33=VDDIO=3.3V)

Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Reference voltage	V_{REF}	Load current = 1.2mA	1.176	1.2	1.224	V

Temperature sensor

*Design assurance items before correction

(Unless otherwise specified, VDD33=VDDIO=3.3V)

Item	Symbol	Condition	Min.	Тур.	Max.	Unit
Temperature sensitivity	T _{Sens}	VREFP = VDD33 = $3.3V$ Ta = -40 ~ +85deg.C	0.25	-	-	mV/ deg.C/VREF
Non-linearity	т	VREFP = VDD33 = 3.3V Ta = -40 ~ +85deg.C	-6	-	6	%FS
	T_{NL}	VREFP = VDD33 = 3.3V Ta = 0 ~ +50deg.C	-4	-	4	%FS

AD convert

*Design assurance items

(Unless otherwise specified, Ta=25deg.C, VDD33=VDDIO=3.3V)

Item	Symbol	Conditions	Min.	Тур.	Max.	Unit
Setting range of data		High Power Mode (HPM)	20	-	2560	Hz
output rate		Low Power Mode (LPM)	10	-	1280	Hz
Differential input impedance	Zdiff_in		1	-	-	MΩ
Differential full scale range	VID,FSR		-VREFP	-	VREFP	V
	V _{noise1}	Data output rate = 2560Hz(HPM)/1280Hz(LPM) VREFP = VDD33 = 3.3V	-	17.61	52.11	
	V _{noise2}	Data output rate = 1280Hz(HPM)/640Hz(LPM) VREFP = VDD33 = 3.3V	-	7.47	13.56	
	V _{noise3}	Data output rate = 640Hz(HPM)/320Hz(LPM) VREFP = VDD33 = 3.3V	-	4.71	7.37	
Input conversion noise	V _{noise4}	Data output rate = 320Hz(HPM)/160Hz(LPM) VREFP = VDD33 = 3.3V	-	3.19	5.10	
voltage	V _{noise5}	Data output rate = 160Hz(HPM)/80Hz(LPM) VREFP = VDD33 = 3.3V	-	2.34	3.60	uVrms
	V _{noise6}	Data output rate = 80Hz(HPM)/40Hz(LPM) VREFP = VDD33 = 3.3V	-	1.74	2.67	
	V _{noise7}	Data output rate = 40Hz(HPM)/20Hz(LPM) VREFP = VDD33 = 3.3V	-	1.29	2.16	
	V _{noise8}	Data output rate = 20Hz(HPM)/10Hz(LPM) VREFP = VDD33 = 3.3V	-	1.05	2.16	
Integral non-linearity	TNU	VREFP = VDD33 = 3.3V Ta = +25 deg.C Common mode voltage = VDD33/2	-30	-	30	ppm Of FSR
	INL	VREFP = VDD33 = 3.3V Ta = -40 ~ +85 deg.C Common mode voltage = VDD33/2	-150	-	150	ppm Of FSR

SERIAL INTERFACE

SPI and I2C of serial communication interface are supported. You can choose SPI (max.: 5Mbps) or I2C (max.: 3.4Mbps) by PSEL-pin. When PSEL-pin is set to High, SPI is selected; when it is Low, I2C. Set the High voltage of PSEL-pin to the same electric potential as that of VDDIO-pin.

Communication speed

*Design assurance items

(Unless otherwise specified, Ta=25deg.C, VDD33=VDDIO=3.3V)

Item	Symbol	Condition	Min.	Тур.	Max.	Unit
I2C communication speed	BR _{I2CHs1}	$\begin{array}{l} \text{VDDIO} \geq 2.0\text{V} \\ \text{Cb} \leq 100\text{pF} \end{array}$	-	-	3.4M	
(Hs mode) BR _{I2CHs2}		$\begin{array}{l} \text{VDDIO} \geq 2.0\text{V} \\ \text{Cb} \leq 400\text{pF} \end{array}$	-	-	1.7M	
I2C communication speed (Fast mode)	BR I2CFm	VDDIO < 2.0V	-	-	400k	bac
	BR _{SPI1}	$\begin{array}{l} \text{VDDIO} \geq 2.0\text{V} \\ \text{Cb} \leq 100\text{pF} \end{array}$	-	-	5.0M	bps
SPI communication speed	BR _{SPI2}	$\begin{array}{l} \text{VDDIO} \geq 2.0\text{V} \\ \text{Cb} \leq 400\text{pF} \end{array}$	-	-	2.5M	
	BR _{SPI3}	VDDIO < 2.0V	-	-	1.0M	

SPI format

SPI command format is shown below. Data transmission is started when CSB becomes low from the status in which SCLK is high. Input data is sampled on rising edges of the SCLK. (SPI MODE 3) For the detailed timing, please refer to each command format.

SPI operation command format

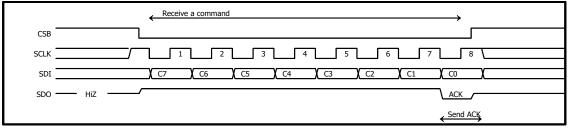


Fig. 10.1 SPI operation command format

SPI result command format

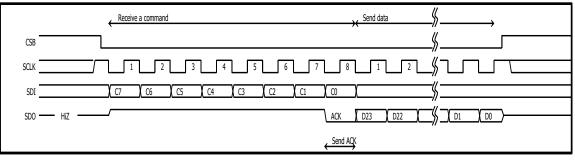


Fig. 10.2 SPI result command format

*The above are the command formats during 24-bit data output. During 8-bit output, it is immediately output from D7 to D0 after ACK transmission.

SPI write (RAM, NVM) command format

Following the command, send 8-bit memory address and writing data. The writing data should be 8 bits for sequencer RAM / NVM and 32 bits for MAC RAM. After receiving a write command, the internal area becomes busy for 50msec at the maximum to write memory. During busy, SDO becomes Low. Please note that all commands are ignored during busy.

How to discern busy:

After sending the writing data, continue to input clock with maintaining communicating mode. Then, 00h indicating busy status is output. When the writing is completed, 01h will be output. *The "00h" indicating busy may sometimes be output or not depending on the clock frequency.

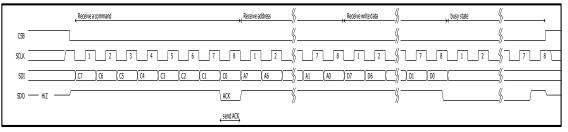


Fig. 10.3 SPI write (RAM, NVM) command format

SPI write (Register) command format

Following the command, send 8-bit memory address and 8-bit write data.

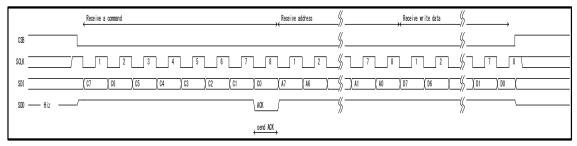


Fig. 10.4 SPI write (Register) command format

SPI read (RAM, NVM) command format

Following the command, send 8-bit memory address. After receiving memory address, the internal area becomes busy for 25usec at the maximum to prepare for data sending. During this time, 00h indicating busy status is output. When data preparation is completed, 01h is output. Continuously, 8-bit data is output for sequencer RAM and NVM, and 32-bit data for MAC RAM.

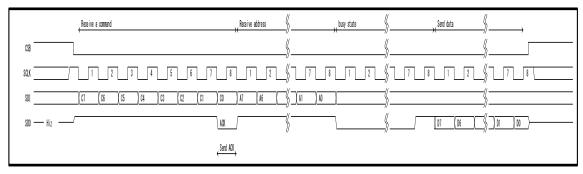


Fig. 10.5 SPI read (RAM, NVM) command format

SPI read (Register) command format

Following the command, send 8-bit memory address. After receiving the memory address, 8-bit data is output.

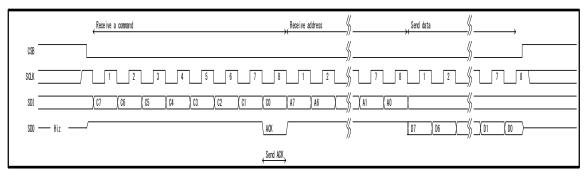


Fig. 10.6 SPI read (Register) command format

SPI AC characteristics



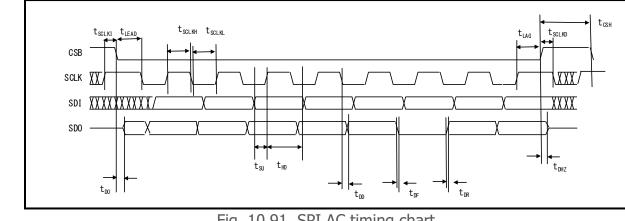


Fig. 10.91 SPI AC timing chart

(Unless otherwise specified, Ta=25deg.C, VDD33=3.3V)

Table 10.1 SPI AC characteristics

Itom	Cumhal	VDDI	0<2V	VDDIC	$0 \ge 2V$	Linit
Item	Symbol	min.	max.	min.	max.	Unit
SCLK frequency (Duty $50 \pm 10\%$)	f _{SCLK}	-	1	-	5	MHz
SCLK High period (90%~90%)	t sclkh	400	-	80	-	ns
SCLK Low period (10%~10%)	tsclkl	400	-	80	-	ns
SCLK standby time	t _{SCLKI}	500	-	100	-	ns
SCLK delay time	tsclkd	0	-	0	-	ns
CSB High period (90%~90%)	tcsн	1000	-	200	-	ns
Time from CSB falling edge to SCLK falling edge	tlead	0	-	0	-	ns
Time from SCLK rising edge to CSB rising edge	tlag	500	-	100	-	ns
SDI setup time	tsu	100	-	10	-	ns
SDI hold time	t _{HD}	10	-	10	-	ns
SDO rise time (Load: 100pF) (10%~90%)	t _{DR}	-	50	-	50	ns
SDO fall time (Load: 100pF) (10%~90%)	t _{DF}	-	50	-	50	ns
SDO output delay time (Load: 100pF)	t _{DD}	-	120	-	60	ns
SDO output delay time (Load: 100pF) from CSB became Low	t _{DO}	-	120	-	60	ns
Time from CSB reaches High to SDO reaches HiZ (Load: 100pF)	t _{DHZ}	-	170	-	170	ns

I2C format

I2C address is composed of total 8 bits: 7 bits of slave-address in the head and the rest 1 bit of R/W bit. Users can set the slave-address (7 bits) of MM3609 optionally by writing to NVM (default 1001111). However, 0000xxx and 1111xxx cannot be used because they are reserved addresses. *Please use this product after confirming I2C specification and understanding the details.

I2C operation command format

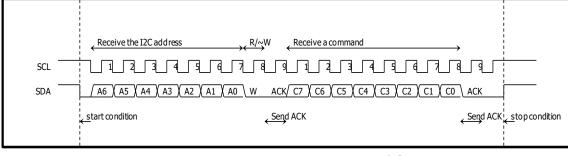


Fig. 10.102 I2C operation command format

I2C result command format

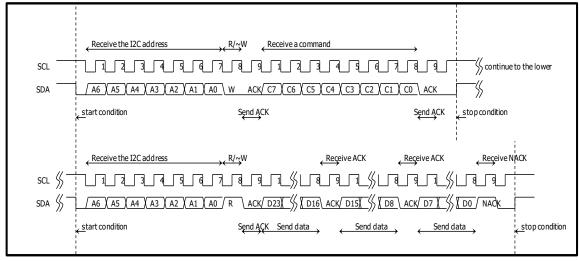


Fig. 10.113 I2C result command format

I2C write (RAM, NVM) command format

Following the command, send 8-bit memory address and writing data. The writing data should be 8 bits for sequencer RAM / NVM and 32 bits for MAC RAM. After receiving a write command, the internal area becomes busy for 50msec at the maximum to write memory. During busy, SCL becomes Low.

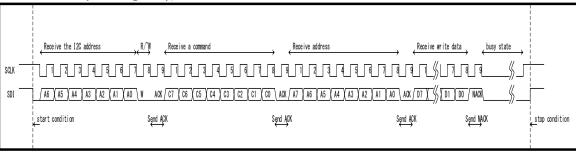


Fig. 10.124 I2C write (RAM, NVM) command format

I2C write (Register) command format

Following the command, send 8-bit memory address and 8-bit writing data.

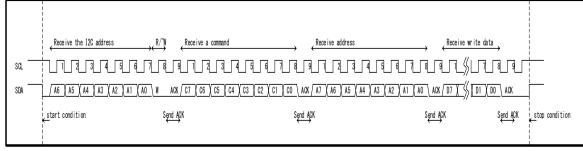


Fig. 10.135 I2C write (Register) command format

I2C read (RAM, NVM) command format

Following the command, send 8-bit memory address. After receiving memory address, it becomes busy during preparation for sending data. During this time, SCL becomes Low. SCL is released when data preparation is completed. Subsequently, when it is accessed (read command is sent) in the read mode, 8-bit data is output for sequencer RAM / NVM and 32-bit data for MAC RAM.

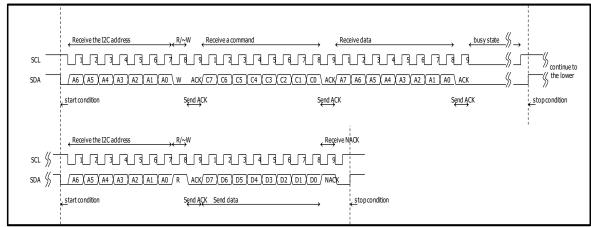


Fig. 10.146 I2C read (RAM, NVM) command format

I2C read (Register) command format

Following the command, send 8-bit memory address. Subsequently, when it is accessed (read command is sent) in the read mode, 8-bit data is output.

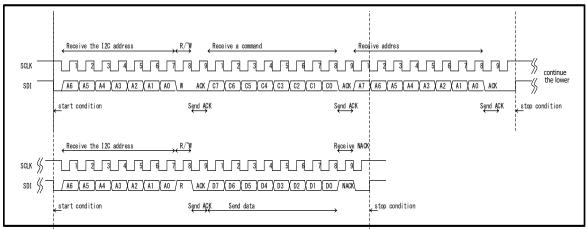


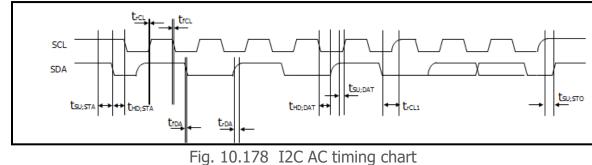
Fig. 10.157 I2C read (Register) command format

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I2C AC characteristics

*Design assurance item



(Unless otherwise specified: Ta=25deg.C, VDD33=3.3V)

Table 10.2 I2C AC characteristics

		VDDIO	< 2.0V		VDDIO	≥ 2.0V		
Item	Symbol	Fact	mode		Hs n	node	Unit	
item	Symbol	Fasi	moue	Cb ≤	100pF	Cb ≤ ·	Cb ≤ 400pF	
		min.	max.	min.	max.	min.	max.	
SCL frequency	f scl	0	400kHz	0	3.4	0	1.7	MHz
Start condition setup time	tsu;sta	600	-	160	-	160	-	ns
Start condition hold time	thd;sta	600	-	160	-	160	-	ns
Stop condition setup time	t _{su;sto}	600	-	160	-	160	-	ns
Data setup time	t _{su;dat}	100	-	20	-	20	-	ns
Data hold time (note ⁷)	thd;dat	20	-	20	70	20	150	ns
SCL rise time	t _{rCL}	-	300	10	40	20	80	ns
Rise time of SCL after ACK (When clock stretch is released.)	t _{rCL1}	-	300	10	80	20	160	ns
SCL fall time	t _{fCL}	10	300	10	-	20	80	ns
SDA rise time	t _{rDA}	-	300	10	80	20	160	ns
SDA fall time	t _{fDA}	10	300	10	80	20	160	ns

note⁷: This product does not have the function to retain data in SDA. Please ensure SDA is held for 20nsec in the area where SCL falling edge is not defined.

Command list

Table 10.3 Operation command list (1/2)Command Code Action Command Name BIN. HEX. C7 C6 C5 C4 C3 C2 C1 C0 Reset the IC. After the reset, 0 0 Reset 0x72 1 1 1 0 1 0 boot loader behaves automatically. 0 0 0 0 0 Shutdown 0x90 1 1 0 Shift to shutdown state Standby 1 0 0 1 0 1 0 Shift to standby state 0x92 0 Idle 1 0 0 1 0 1 0 0 Shift to idle state 0x94 Shift to Active state. If this command is output durina Shutdown state, Standby state or Idle state, 0xA0 this IC starts sequence 0xA2 1 0 1 0 0 CM1 CM0 0 automatically. Even if input of 0xA4 active command is continued, 0xA6 this IC does not re-start. To restart, output the active command after shifting the IC Active to shutdown state. C2 and C1 assign AD conversion mode. The values written in 7Ah to 7Dh of NVM are referred for the advanced setting of each mode. CM1 CM0 Conversion mode Description 0 0 Mode 0 AD conversion mode 0 1 0 Mode 1 AD conversion mode 1 1 0 Mode 2 AD conversion mode 2 1 1 Mode 3 AD conversion mode 3

Command Name	HEX.	BIN.							Action	
	HLX.	C7	C6	C5	C4	C3	C2	C1	C0	
	0xB0 0xB2 0xB4 0xB6	1	0	1	1	0	BA1	BA0	0	Convert the banks of NVM. If the command is output during standby or idle state, this IC becomes reset state until boot loader starts automatically.
BankSW	C2 and C1 a	assign th	e bank							
Daliksw	BA1	BA0	BA0 Bank Type				Description			
	0	0		Ban	k 0		Use only bank 0			
	0	1		Ban	k 1		Use only bank 1			
	1	0		Ban	k 2		Use only	/ bank 2		
	1	1	1 Bank wrapper		Use the latest data of bank 0 to 3					
	<u>_</u>		•							

Table 10.4 Operation command list (2/2)

			Сс	ommar	nd Cod	е				
Command Name	HEX.				В	IN.				Action
	HEA.	C7	C6	C5	C4	C3	C2	C1	C0	
	0xC0 0xC2 0xC4 0xC6	1	1	0	0	0	D1	D0	0	Read the result of sequencer calculation.
Result	The data is negative nu and convert Sequencer (C2 and C1 assign the result of AD-conversion. The data is output in the forms of 24 bits and MSB 1 st . This IC uses two's complement to express negative number. If you want to obtain Result0 as a relative value, input reference value to result2 and convert AD. The reference value is the copied value of Result 0 which is a standard by using Sequencer Command Cal Copy. Default value of Result2 is 0.								
	D1	D0	D0 AD convert result Description					_		
	0	0	0 Result 0 Output physical sensor value.							
	0	1	1 Result 1 Output temperature sensor value.							
	1	0		Resu	ult 2		Output value.	referenc	e	
	1	1		Resu	ult 3		Reserv	е]
	0x80	1	0	0	0	0	0	0	0	Output status signals that can indicate the IC status.
	Output 8-bit data depending on the conditions								-	
	D7 D6				D2 D		00	State		-
Status	0 0 1 1	0 0							4	
	1 1	1 (-	-)	1 Id	/		4
	1 1	1 ()		tive		1
		I `				I				_

Table 10.51 Result con	mmand list
------------------------	------------

		Tubic	10.02	. INCO	u / w		omman	iu iist			
			C	ommar	nd Cod	e					
Command Name		BIN.							Action		
	HEX.	C7	C6	C5	C4	C3	C2	C1	C0		
Read	0xD0 0xD2 0xD4 0xD6	1	1	0	1	0	M1	M0	0	Read data from NVM, register and RAM.	
Write	0xE0 0xE2 0xE4 0xE6	1	1	1	0	0	M1	M0	0	Write data to NVM, register and RAM.	
	Assign the	type of r	nemor	y with	M1 an	d M0.				·	
	M1	M0	Т	ype of	Memo	ory		of data nd rece		ing	
Dood/W/rito	0	0		Reg	jister		8 bit				
Read/Write	0	1	1 Sequencer RAM		8 bit						
	1	0	0 MAC RAM		32 bit (Low 28 bit)						
	1	1					8 bit				

Table 10.62 Read / write command list

State

State								
Plack		Sta						
Block	Shutdown	Standby	Idle Boot Load	Active				
Digital Block(VDDIO)	ON	ON	ON	ON				
Digital Block(1.2VREG)	OFF	ON	ON	ON				
Oscillator	OFF	OFF	ON	ON				
Sequencer	OFF	OFF	OFF	ON				
NVM	OFF	OFF	ON	ON (note ⁸)				

Table 10.7 State definition list

State transition

Table 10.8 State transition list

Dessiving command		Sta	ate	
Receiving command	Shutdown	Standby	Idle	Active
Reset	O Shift to Shutdown after Reset and BootLoad	O Shift to Shutdown after Reset and BootLoad	O Shift to Shutdown after Reset and BootLoad	O Shift to Shutdown after Reset and BootLoad
Status	O Keep Shutdown	O Keep Standby	O Keep Idle	O Keep Active
Shutdown	×	O Shift to Shutdown	O Shift to Shutdown	O Shift to Shutdown
Standby	O Shift to Standby after Reset and BootLoad	×	O Shift to Standby	Not supported (note ⁹¹)
Idle	O Shift to Idle after Reset and BootLoad	O Shift to Idle	×	O Shift to Idle
Active	O Shift to active after Reset and BootLoad Implement sequence *The destination to shift depends on sequence.	O Shift to Active Implement sequence *The destination to shift depends on sequence.	O Shift to Active Implement sequence *The destination to shift depends on sequence.	×
Bank SW	O Keep Shutdown	O Back to Standby after Reset and BootLoad	O Back to Idle after Reset and BootLoad	O Keep Active *The destination to shift depends on sequence.
Result	×	0	0	0
Read	×	△ Only register is acceptable.	0	Not supported (note ⁸)
Write	×	△ Only register is acceptable.	0	Not supported (note ⁸)

O:Accept ×:Ignore

note⁸: Although command is acceptable, it goes unintended behavior since sequence is running.

note⁹: If you want to shift the state from active to standby, please issue standby command after issuing idle command.

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After turning on the power, POR circuit built in this IC resets digital circuit. After resetting, it conducts boot load and reads the contents of NVM to a register and RAM. There are Boot Load 0 that reads I2C address etc. and Boot Load 1 that reads sequence program, correction value, etc. After Boot Load0, this IC shifts to the Shutdown state. When receiving a command from host, after shifting to Boot Load1, the IC shifts to the Standby state, Idle state, and active state following to the command. By writing to the auto-start acceptance setting to NVM, after turning on the power, this IC can be shifted to Boot Load0, Boot Load1, and active state.

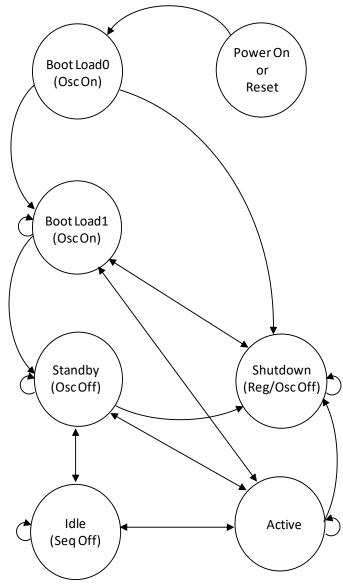


Fig. 10.18 State transition diagram

NVM (Non-volatile memory)

MM3609 contains NVM (Non-volatile memory) in order to store sensor correction value and sequence program. NVM is OTP (One-Time Programmable) where data cannot be erased once it is written in. The 4k bits are divided into four banks. This configuration allows you to write to each area of 1k bit, this can be used as a FTP(Few-Times Programmable) on which can be written for four times, although it is OTP.

If you want to use multiple sequence programs, this product can apply to multiple applications by writing different sequence programs on each bank and selecting the bank to use for BsnkSW command. The newest I2C address shold be used at all times.

NVM Address Map

Addr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0		
00h	Reserve	Assign shift state after Boot Load	state after Reserve Boot Load							
01h	Reserve			IZ	2C Address[6:	0]				
02h ~ 06h		Reserve								
07h				Res	serve					
08h ~ 47h	Sequence p	rogram 00h to	3Fh							
48h ~ 50h	External ser coefficient	nsor offset ten	nperature cha	aracteristics	zero-order co	efficient, prim	ary coefficier	nt, secondary		
51h ~ 59h		External sensor primary change temperature characteristics zero-order coefficient, primary coefficient, secondary coefficient								
5Ah ~ 62h		External sensor secondary change temperature characteristics zero-order coefficient, primary coefficient, secondary coefficient								
63h ~ 6Eh		coefficient for oefficient, terti				hange correct	ion coefficien	t, secondary		
6Fh ~ 77h	reserve coe	fficient1, reser	ve coefficient	2, reserve coe	efficient3					
706		Rese	erve		A1 sensor	type [1:0]	A0 sensor	type [1:0]		
78h	Kind of sense	sor: 0, not con	nected; 1, ph	ysical sensor;	2, temperatu	re sensor				
		Temp	Result Bit Shi	ft[2:0]		Phy F	Result Bit Shift	t[2:0]		
79h	Reserve	Assign the quantity of bit shift of the Assign the quantity of the bit shift of								
	Mode 0 te	mperature sen	sor CIC decin	nation ratio	Mode 0	Physical sense	or CIC decima	tion ratio		
7Ah ~ 7Dh		mperature sen				, Physical sense				
7An ~ 7Dh		mperature sen				Physical sense				
	Mode 3 te	Mode 3 temperature sensor CIC decimation ratio Mode 3 Physical sensor CIC decimation ratio								
7Eh ~ 7Fh			Chec	k some area:	CRC16CCITT	[15:0]				

80h	Reserve
81h ~ FFh	Bank1 address 01h to 7Fh
	·

100h	Reserve
101h ~ 17Fh	Bank2 address 01h to 7Fh

180h	Reserve
181h ~ 1FFh	Bank3 address 01h to 7Fh

REGISTER

The resisters of this product are a result resister where the result of correction calculation is stored, and register where control register to control IC is aligned. This has 8-bit width.

Register address map

Table 12.1 Register address map								
Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
[Result Register	[Result Register]							
00h ~02h	The bit shift Result 0 cor *The bit shi First, please	Calculated result of physical quantity of corrected and proofed external sensor 0 (24bit) The bit shifted value is that stored in the 75h address of MACRAM. Result 0 command reads this data. *The bit shift quantity is assigned by the address 79h of NVM. Default 0 = Right 4 bit shift First, please read 00h address. Next, please read until 02h address.						
03h ~05h	The bit shift Result 1 cor *The bit shi	Calculated result of corrected temperature value (24bit) The bit shifted value is that stored in the 74h address of MACRAM Result 1 command reads this data. *The bit shift quantity is assigned by the address 79h of NVM. Default 0= Right 4 bit shift First, please read 03h address. Next, please read until 05h address.						
06h ∼08h	The bit shift Result 2 cor ※The bit sh	Corrected External sensor0 physical quantity standard value (24bit) The bit shifted value is that stored 76h address of MACRAM. Result 2 command reads this data. %The bit shift quantity is assigned by the address 79h of NVM. Default 0 = Right 4 bit shift First, please read 06h address. Next, please read until 08h address.						
09h ~0Bh	Reserve for calculation 15(24bit) The bit shifted value is that stored in 7Ah address of MACRAM. Result 3 command reads this data. *The bit shift quantity is assigned by the address 79h of NVM. Default 0 = right 4 bit shift First, please read 09h address. Next, please read until 0Bh address.							
0Ch ∼0Fh	ADC (CIC filter, FIR filter) output value First, please read 0Ch address. Next, please read until 0Fh address.							
10h ~20h	L'aconvo							
[Control Register]								
21h ~3Eh	Reserve							
	Reserve						CMD1	CMD0
3Fh	CMD1,CMD0 This bit is re		Until Ctrl Reg	g 3Fh [1, 0] in	sequence cor	mmand and Ju	ump If Ctrl Reg	3Fh [1, 0].
40h ~53h	L'ACONIO							

MAC RAM (Multiply and ACcumulation RAM)

This RAM is for MAC (Multiply and ACcumulation). This RAM is used for calculations of sequence command. This has 28-bit width.

MAC RAM address map

Address	Description
[FIR Filter Settir	nal
00h ~	
3Eh	FIR tap 00~62
3Fh	Reserve
40h ~	Reserve
5Fh	I CESEI VE
[Compensation	Coefficient]
60h	External sensor offset correction coefficient temperature zero-order coefficient
61h	External sensor offset correction coefficient temperature primary coefficient
62h	External sensor offset correction coefficient temperature secondary coefficient
63h	External sensor primary correction coefficient temperature zero-order correction coefficient
64h	External sensor primary correction coefficient temperature primary correction coefficient
65h	External sensor primary correction coefficient temperature secondary correction coefficient
66h	External sensor secondary correction coefficient temperature zero-order correction coefficient
67h	External sensor secondary correction coefficient temperature primary correction coefficient
68h	External sensor secondary correction coefficient temperature secondary correction coefficient
69h	Temperature sensor temperature zero-order coefficient
6Ah	Temperature sensor temperature primary coefficient
6Bh	Temperature sensor temperature secondary coefficient
6Ch	Temperature sensor temperature tertiary coefficient or preparatory coefficient 0
6Dh	Reserve coefficient 1
6Eh	Reserve coefficient 2
6Fh	Reserve coefficient 3
	compensation, arithmetic]
70h	ADC (CIC filter, FIR filter) output value
71h	Computed result of offset correction coefficient of external sensor of the current temperature
72h	Computed result of primary sensitivity correction coefficient of external sensor under current temperature
73h	Computed result of secondary sensitivity correction coefficient of external sensor under current
	temperature
74h	Computed result of Corrected temperature value
75h	Computed result of physical quantity of corrected and proofed external sensor0
76h	Standard value of physical quantity of corrected external sensor0
77h	Reserve for calculation 12
78h	Reserve for calculation 13
79h	Reserve for calculation 14
7Ah	Reserve for calculation 15
7Bh	Reserve
7Ch	Reserve
7Dh	Reserve
7Eh	Reserve
7Fh	Reserve

Table 13.1 MAC RAM address map

SEQUENCER RAM

The maximum quantity of sequence program is 64 bytes. This IC copies the sequence program written on NVM to this area during Boot Load. This has 8-bit width.

Sequencer RAM address map

Table 14.1 Sequencer RAM address map

Address	Description
00h ~ 3Fh	Sequence program

SEQUENCER

Sequencer is a function that can implement sequence program stored in NVM in order. This can control behaviors of sensor, ADC, digital filter, correction calculation, and output-interrupt signals. This is also able to program the loop structure include finish judgment. For a judgment of finish, you can choose one from interruption by host, interruption from internal IC or designation of loop frequency up to 15 times.

The maximum capacity of sequence program is 64 bytes. The command code is one byte. Parameter of one to two bytes is required depending on the command.

Sequence command group list

	Table 15.1	Sequence	command	group	list ((Basic)	
--	------------	----------	---------	-------	--------	---------	--

Group name *Linked to the detailed command list	Group Description
Init/Copy	Initialization, copy
Power Mode	Power Mode setting
Set Ref Current	Output current setting of IS pin
Block Enable	Enable the settings of each circuit block
Block Disable	Disable the settings of circuit block
Compensation	Compensation calculation
Bit Shift	Zero to 15bit shift from side to side
[GPO Output(SDO,GPO0)]	Output setting of GPO
Wait	Wait control
Loop/Jump	Sequence flow control
End	Completed

Table 15.2 Sequence command group list (Advanced)

Group name *Linked to detailed command list	Group Description
DSM WarmUp Setting	Setting of start wait of $ ightarrow \Sigma$ modulator
FIR Filter	FIR filter ON/OFF, settings of decimation ratio
Arithmetic	Calculation for general purpose

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Details of sequence command

Table 15.3 Details of sequence command (Basic)

	Table 15.5 Details of sequence command (basic)		
Code	ode Command Description		
[Init/Cop	ſvi		
01h	Clear Temp Data	Clear the address of MAC RAM 0x71 to 0x74	
02h	Clear FIR Result	Clear the address of MAC RAM 0x00 to 0x5F	
03h	Clear MAC Result	Clear the address of MAC RAM 0x70 to 0x7F	
04h	Clear MAC RAM	Clear the address of MAC RAM 0x00~0x7F	
05h	Set PhyVal to PhyCal	Copy MAC RAM 0x75 to 0x76	
06h	Copy MAC RAM Data AtoB	Copy MAC RAM data from the designated address to the designated	
	Parameter 1:srcA_addr[7:0]	address.	
		Source address (8bit)	
	Parameter 2:dstB_addr[7:0]	Designate MACRAM Address from 0x00 to 0x7F	
		Destination address (8bit)	
		Designate MACRAM Address from 0x00 to 0x7F	
2Ch	Save Temporary	Save MAC RAM 0x74~0x76 and 0x7E~0x7F to the area where values	
		can be maintained even though they are in Shutdown State.	
2Dh	Load Temporary	Load MAC RAM 0x74~0x76 and 0x7E~0x7F from the saved area	
[Power N	1ode]		
08h	High Power Mode	Set DSM to HPM (High Power Mode)	
09h	Low Power Mode	Set DSM to LPM(Low Power Mode) (Default)	
[Set Ref	Current]		
11h	IS Output Current	Set current value of IS-pin	
1111	Parameter 1: RefCurrent[7:0]	Reference current (8bit)	
		00h:OFF	
		01h:10uA ~ 7Fh:1270uA	
		×10uA step	
31h	IS Output Current 0	Set the current value of IS-pin to zero	
[Block Er			
10h	EN IS	Enable IS-pin	
1011		Output the current set by Is Output Current (11h) command to IS-pin	
12h	EN A0 Sensor	Enable COM0 and MUX Ch0	
1211	(COM0, MUX Ch0 ON)		
13h	EN A1 Sensor	Enable COM1 and MUX Ch1	
	(COM1, MUX Ch1 ON)		
14h	EN Temp Sensor	Enable Internal Temperature Sensor and MUX Ch2.	
	(Int Temp Sensor, MUX Ch2 ON)		
18h	EN DSM & Wait for Conversion	Enable DSM, CIC Filter and FIR Filter.	
		Start AD conversion. Wait until the conversion completed.	
28h	EN VREFBUF	Enable VREFBUF	
		Output VREFBUF 1.2V to VREFP-pin	
[Block Di	isable]		
30h	DIS IS	Disable IS-pin	
32h	DIS COM0,MUX HiZ	Disable COM0 and MUX (HiZ)	
33h	DIS COM1,MUX HIZ	Disable COM1 and MUX (HiZ)	
34h	DIS Int Temp Sensor, MUX HiZ	Disable Internal Temp Sensor and MUX (HiZ)	
38h	DIS DSM	Disable DSM, CIC Filter, and FIR Filter	
39h	DIS VREFBUF	Disable VREFBUF	

[Compen	sation]	
19h	Compensation 2D Internal Temp Sensor	Compensation 2D Internal Temperature Sensor (Bit shift enable)
1Ah	Compensation 3D Internal Temp Sensor	Compensation 3D Internal Temperature Sensor (Bit shift enable)
1Bh	Compensation Phy Sensor 2D Sensitivity	Compensation Physical Sensor 2D Sensitivity (Bit shift enable)
1Ch	Compensation Phy Sensor 1D Sensitivity	Compensation Physical Sensor 1D Sensitivity (Bit shift enable)
1Dh	Compensation Phy Sensor Offset	Compensation Physical Sensor Offset (Bit shift enable)
1Eh	Compensation External Sensor	Compensation External Sensor (Bit shift enable)
[Bit Shift]	· · ·	
		calculated result preliminary. A bit shift which is set after conducting
	on command for bit shift enable is conduct	
90h	Bit Shift Cancel	Bit Shift Cancel (Default)
91h	Right 1bit Shift	Right 1bit Shift
92h	Right 2bit Shift	Right 2bit Shift
93h	Right 3bit Shift	Right 3bit Shift
94h	Right 4bit Shift	Right 4bit Shift
95h	Right 5bit Shift	Right 5bit Shift
96h	Right 6bit Shift	Right 6bit Shift
97h	Right 7bit Shift	Right 7bit Shift
98h	Right 8bit Shift	Right 8bit Shift
99h	Right 9bit Shift	Right 9bit Shift
9Ah	Right 10bit Shift	Right 10bit Shift
9Bh	Right 11bit Shift	Right 11bit Shift
9Ch	Right 12bit Shift	Right 12bit Shift
9Dh	Right 13bit Shift	Right 13bit Shift
9Eh	Right 14bit Shift	Right 14bit Shift
9Fh	Right 15bit Shift	Right 15bit Shift
A0h	Bit Shift Cancel	Bit Shift Cancel
A1h	Left 1bit Shift	Left 1bit Shift
A2h	Left 2bit Shift	Left 2bit Shift
A3h	Left 3bit Shift	Left 3bit Shift
A4h	Left 4bit Shift	Left 4bit Shift
A5h	Left 5bit Shift	Left 5bit Shift
A6h	Left 6bit Shift	Left 6bit Shift
A7h	Left 7bit Shift	Left 7bit Shift
A8h	Left 8bit Shift	Left 8bit Shift
A9h	Left 9bit Shift	Left 9bit Shift
AAh	Left 10bit Shift	Left 10bit Shift
ABh	Left 11bit Shift	Left 11bit Shift
ACh	Left 12bit Shift	Left 12bit Shift
ADh	Left 13bit Shift	Left 13bit Shift
AEh	Left 14bit Shift	Left 14bit Shift
AFh	Left 15bit Shift	Left 15bit Shift
	tput(SDO,GPO0)]	
	PI communication, the settings of SDO-pin	s are disabled.
COh	GPO 0,0	Set SDO-pin, Low; GPO0-pin, Low
C1h	GPO 0,1	Set SDO-pin, Low; GPO0-pin, High (Default)
C4h	GPO 1,0	Set SDO-pin, High; GPO0-pin, Low
C5h	GPO 1,1	Set SDO-pin, High; GPO0-pin, High
0.511		

[Wait]				
40h	Wait 100usec	Wait 100usec		
41h	Wait 500usec	Wait 500usec		
42h	Wait 1msec	Wait 1msec		
43h	Wait 5msec	Wait 5msec		
44h	Wait 10msec	Wait 10msec		
45h	Wait 50msec	Wait 50msec		
46h	Wait 100msec	Wait 100msec		
47h	Wait 500msec	Wait 500msec		
4Bh	Wait Until FIR/CIC Finished	Wait Until FIR/CIC filter Finished		
4Dh	Wait Until Result Command	Wait until receiving result command		
ibii		*This command is available for only once combined with Jump Detect		
		Result Command within a same sequence.		
4Eh	Wait Until Ctrl Reg 3Fh[1]=1	Wait until 3Fh[1] of control register to be High		
4Fh	Wait Until Ctrl Reg 3Fh[0]=1	Wait until 3Fh[0] of control register to be High		
[Loop/Ju				
	Common parameter	Turner address (Phit)		
	Parameter 1:JumpAddr[7:0]	Jump address (8bit)		
E1b	Jump Lintil MAC Compare TRUE	Designate the sequence address from 00h to 3Fh		
54h	Jump Until MAC Compare TRUE	Jump Until the result of comparing calculation is true.		
55h	Jump Until Detect Result Command	Jump Until Result command is received. *This command is available for only once combined with Wait Until		
56h	Jump Until Ctyl Dog 256[1] 1	Result Command within a same sequence		
57h	Jump Until Ctrl Reg 3Fh[1]=1	Jump Until control register 3Fh [1] is High		
	Jump Until Ctrl Reg 3Fh[0]=1	Jump Until control register 3Fh [0] is High.		
58h 59h	Infinite Loop	Unconditional Jump (Effective number: Unlimited)		
	1-time Loop	Unconditional Jump (Effective number: Once)		
5Ah	2-time Loop	Unconditional Jump (Effective number: Twice)		
5Bh	3-time Loop	Unconditional Jump (Effective number: Three times)		
5Ch	4-time Loop	Unconditional Jump (Effective number: Four times)		
5Dh	5-time Loop	Unconditional Jump (Effective number: Five times)		
5Eh	6-time Loop	Unconditional Jump (Effective number: Six times)		
5Fh	7-time Loop	Unconditional Jump (Effective number: Seven times)		
60h	8-time Loop	Unconditional Jump (Effective number: Eight times)		
61h	9-time Loop	Unconditional Jump (Effective number: Nine times)		
62h	10-time Loop	Unconditional Jump (Effective number: Ten times)		
63h	11-time Loop	Unconditional Jump (Effective number: 11 times)		
64h	12-time Loop	Unconditional Jump (Effective number: 12 times)		
65h	13-time Loop	Unconditional Jump (Effective number: 13 times)		
66h	14-time Loop	Unconditional Jump (Effective number: 14 times)		
67h	15-time Loop	Unconditional Jump (Effective number: 15 times)		
[End]				
00h	End (transition to idle)	Sequence completed *After sequence is completed, shift to idle state		
36h	End (transition to standby)	Sequence completed *After sequence is completed, shift to standby state		
37h	End (transition to shutdown)	Sequence completed *After sequence is completed, shift to shutdown state		

Code	Command	Description	
[DSM Wa	rmUp Setting]		
0Ah	DSM Start Wait Setting	Set the default no-output period and wait time of modulator	
	Parameter 1(higher 2bit):	Initial no-output period (2bit)	
	non-OutputCount[7:6]	00:1 decimation	
	, 2 2	01:2 decimation	
		10:3 decimation (default)	
		11:4 decimation	
	Parameter 1(lower 6bit):	Wait time (6bit)	
	WarmUpCount[5:0]	00_0000:0 modulation clock	10_0000:128 modulation clock
		00_0001:1 modulation clock	10_0001:256 modulation clock
		00_0010:2 modulation clock	10_0010:384 modulation clock
		00_0011:3 modulation clock	10_0011:512 modulation clock
		00_0100:4 modulation clock	10_0100:640 modulation clock
		00_0101:5 modulation clock	10_0101:768 modulation clock
		00_0110:6 modulation clock	10_0110:896 modulation clock
		00_0111:7 modulation clock	10_0111:1024 modulation clock
		00_1000:8 modulation clock	10_1000:1152 modulation clock
		00_1001:9 modulation clock	10_1001:1280 modulation clock
		00_1010:10 modulation clock (Default)	10_1010:1408 modulation clock
		00_1011:11 modulation clock	10_1011:1536 modulation clock
		00_1100:12 modulation clock	10_1100:1664 modulation clock
		00_1101:13 modulation clock	10_1101:1792 modulation clock
		00_1110:14 modulation clock	10_1110:1920 modulation clock
		00_1111:15 modulation clock	10_1111:2048 modulation clock
		01_0000:16 modulation clock	11_0000:2176 modulation clock
		01_0001:17 modulation clock	11_0001:2304 modulation clock
		01_0010:18 modulation clock	11_0010:2432 modulation clock
		01_0011:19 modulation clock 01 0100:20 modulation clock	11_0011:2560 modulation clock 11 0100:2688 modulation clock
		01_0101:21 modulation clock	11_0101:2816 modulation clock
		01_0110:22 modulation clock	11 0110:2944 modulation clock
		01 0111:23 modulation clock	11 0111:3072 modulation clock
		01 1000:24 modulation clock	11_1000:3200 modulation clock
		01_1001:25 modulation clock	11_1001:328 modulation clock
		01 1010:26 modulation clock	11 1010:3456 modulation clock
		01_1011:27 modulation clock	11_1011:3584 modulation clock
		01 1100:28 modulation clock	11 1100:3712 modulation clock
		01 1101:29 modulation clock	11 1101:3840 modulation clock
		01_1110:30 modulation clock	11_1110:3968 modulation clock
		01_1111:31 modulation clock	11_1111:4096 modulation clock
[FIR Filte	r]		
78h	FIR Off	Set FIR filter off (Default)	
79h	FIR Decimation Ratio 2	Set decimation ratio of FIR filter "2"	
7Ah	FIR Decimation Ratio 4	Set decimation ratio of FIR filter "4"	
7Bh	FIR Decimation Ratio 8	Set decimation ratio of FIR filter "8"	

Table 15.4 Details of sequence command (Advanced)

Code		Command	Description					
	[Arithmetic]							
These Total the and de	These are general-purpose calculation commands. One byte is needed for command code and two bytes for parameter. Total three bytes are needed. Set Variable Number A which is subject to command code, next, Variable Number B and C, and designate the save destination D and the calculation method before conducting the calculation. Example) Add the offset of reserve coefficient 1 to compensated change-value of external sensor.							
	CodeParameter8AhA: Calculation target		Details					
			Corrected external sensor conversion resu	llt				
			Fixed value 1					
	02h		reserve coefficient1					
				.14				
	A1h							
		Calculation method	D=A*B+C					
	C: Variable 2		Use A 'b+CVariable B for multiplication, division and0000: Fixed value 10001: MACRAM Addr=6Ch0010: MACRAM Addr=6Eh0100: MACRAM Addr=76Fh0110: MACRAM Addr=71h0111: MACRAM Addr=72hVariable C for addition and comparison (0000: Fixed value 00001: MACRAM Addr=6Ch0010: MACRAM Addr=6Ch0010: MACRAM Addr=6Eh0101: MACRAM Addr=70h0111: MACRAM Addr=71h0111: MACRAM Addr=72hDestination D to save calculation results0000: Prohibited setting0001: MACRAM Addr=6Ch0101: MACRAM Addr=6Ch0110: MACRAM Addr=72hDestination D to save calculation results0000: Prohibited setting0001: MACRAM Addr=72hDestination D to save calculation results0000: Prohibited setting0011: MACRAM Addr=6Ch0110: MACRAM Addr=70h0111: MACRAM Addr=71h0111: MACRAM Addr=72hCalculation method (4bit)0000: Multiplication and AdditionD=A*B+C0001: Multiplication and AdditionD=A*B-C0010: Multiplication and Addition	1000: MACRAM Addr=73h 1001: MACRAM Addr=74h 1010: MACRAM Addr=75h 1011: MACRAM Addr=76h 1100: MACRAM Addr=77h 1101: MACRAM Addr=78h 1110: MACRAM Addr=78h 1111: MACRAM Addr=73h 1000: MACRAM Addr=74h 1001: MACRAM Addr=75h 1011: MACRAM Addr=77h 1100: MACRAM Addr=77h 1101: MACRAM Addr=78h 1110: MACRAM Addr=78h 1110: MACRAM Addr=79h 1111: MACRAM Addr=79h 1111: MACRAM Addr=74h				
			0010: Multiplication and Addition D=-A*B+C 0011: Multiplication and Addition D=-A*B-C 0100: Division D=A/B *Disregard C 0101: Comparison operation for Jump command A<=B *Disregard C and D	If C<=A<=B, D=A If A <c, d="C<br">If B<a, d="B<br">1000~1111: Prohibited settings</a,></c,>				

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80h	A=1(Const Value)	Set fixed value 1 to Variable A (Bit shift enable)		
81h	A=Variable 0	Set MACRAM Addr=6Ch to Variable A (Bit shift enable)		
	(MACRAM Addr=6Ch)			
82h	A=Variable 1	Set MACRAM Addr=6Dh to Variable A (Bit shift enable)		
	(MACRAM Addr=6Dh)			
83h	A=Variable 2	Set MACRAM Addr=6Eh to Variable A (Bit shift enable)		
	(MACRAM Addr=6Eh)			
84h	A=Variable 3	Set MACRAM Addr=6Fh to Variable A (Bit shift enable)		
	(MACRAM Addr=6Fh)			
85h	A=FIR Filter Value	Set MACRAM Addr=70h to Variable A (Bit shift enable)		
0.61	(MACRAM Addr=70h)			
86h	A=Phy Sensor Offset Coeff	Set MACRAM Addr=71h to Variable A (Bit shift enable)		
076	(MACRAM Addr=71h)			
87h	A=Phy Sensor 1 st Order Coeff (MACRAM Addr=72h)	Set MACRAM Addr=72h to Variable A (Bit shift enable)		
88h	A=Phy Sensor 2 nd Order Coeff	Set MACRAM Addr=73h to Variable A (Bit shift enable)		
0011	(MACRAM Addr=73h)	Set MACKAM AUU -7511 to Valiable A (bit shift eliable)		
89h	A=Corrected Temp Value	Set MACRAM Addr=74h to Variable A (Bit shift enable)		
0.511	(MACRAM Addr=74h)	Set MACINAM Addi = 7 m to Variable A (bit shint chable)		
8Ah	A=Corrected Phy Value	Set MACRAM Addr=75h to Variable A (Bit shift enable)		
	(MACRAM Addr=75h)			
8Bh	A=Corrected & Cal Phy Value	Set MACRAM Addr=76h to Variable A (Bit shift enable)		
	(MACRAM Addr=76h)			
8Ch	A=Variable12	Set MACRAM Addr=77h to Variable A (Bit shift enable)		
	(MACRAM Addr=77h)			
8Dh	A=Variable13	Set MACRAM Addr=78h to Variable A (Bit shift enable)		
	(MACRAM Addr=78h)			
8Eh	A=Variable14	Set MACRAM Addr=79h to Variable A (Bit shift enable)		
	(MACRAM Addr=79h)			
8Fh	A=Variable15	Set MACRAM Addr=7Ah to Variable A (Bit shift enable)		
	(MACRAM Addr=7Ah)			

Example of application circuit

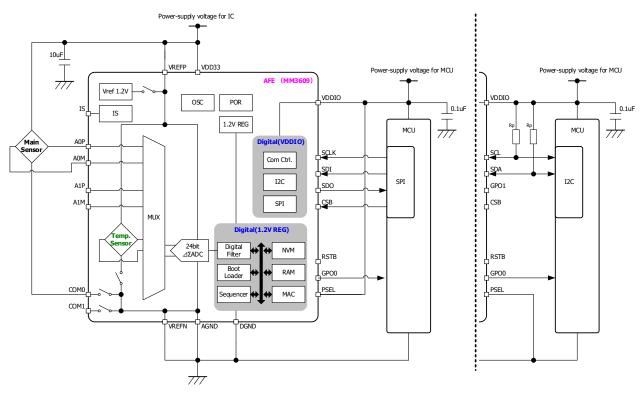


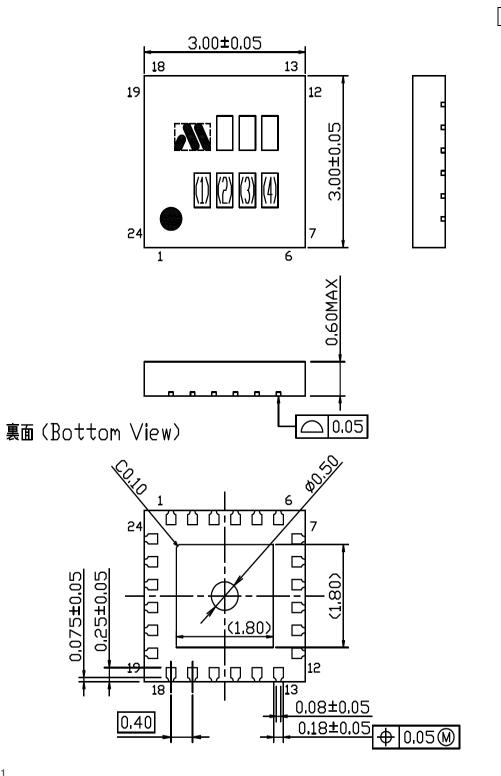
Fig. 16.1 Example of application circuit

OUTLINE DRAWING

PACKAGE: PLP-24A

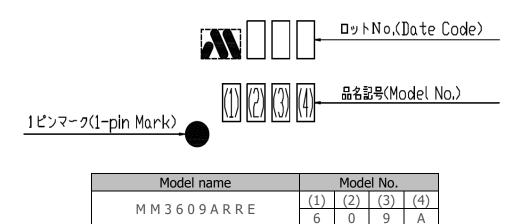
mm

UNIT

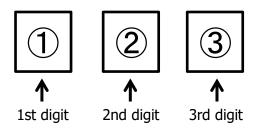


No. R24-PLP24A-0001

MARKING



How to identify 3-digit lot numbers



- 1. The 1st digit (1) shows the last digit of a production year (western calendar).
- 2. The 2nd (2) and 3rd (3) digits show a production week of mass production.

[How to indicate a production year]

The 1st digit (①)				
the last digit of a production	mark			
year				
xxx1	1			
xxx2	2			
xxx3	3			
xxx4	4			
xxx5	5			
xxx6	6			
xxx7	7			
xxx8	8			
xxx9	9			
xxx0	0			

The 2nd and 3rd digit (23)						
production week	mark	production week	mark			
1	01	27	27			
2	02	28	28			
3	03	29	29			
4	04	30	30			
5	05	31	31			
6	06	32	32			
7	07	33	33			
8	08	34	34			
9	09	35	35			
10	10	36	36			
11	11	37	37			
12	12	38	38			
13	13	39	39			
14	14	40	40			
15	15	41	41			
16	16	42	42			
17	17	43	43			
18	18	44	44			
19	19	45	45			
20	20	46	46			
21	21	47	47			
22	22	48	48			
23	23	49	49			
24	24	50	50			
25	25	51	51			
26	26	52	52			
		53	53			

NOTES

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 corresponding to the temperature and designed lifetime after confirming our individual reliability documents (such as
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- Environment with high temperature or high humidity where dew condensation may occur
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MITSUMI ELECTRIC CO., LTD.

Strategy Engineering Department Semiconductor Business Division

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